ABSTRACT OF THE DISCLOSURE

An alignment mark structure (22) for aligning a mask with prior formed features of in a circuit region when an opaque material layer (88) covers the alignment mark structure (22) is provided. The features of the alignment mark structure (22) are formed in an alignment mark region (20) concurrently while features for a circuit region having vertical gate transistors are being formed. There are no extra or added processing steps added for forming the alignment mark structure (22) because it is formed concurrently while forming features in the circuit region. The resulting alignment mark structure (22) has step features (62) so that the step features (62) can be seen after the opaque material layer (88) covers the alignment mark structure (22).